Parallel 16-Bit Rail-to-Rail Micropower DAC

FEATURES

- **16-Bit Monotonic Over Temperature**
- **Deglitched Rail-to-Rail Voltage Output: 8nV•s**
- 5V Single Supply Operation
- I_{CC}: 650µA Typ
- Maximum DNL Error: ±1LSB
- Settling Time: 20µs to ±1LSB
- Internal or External Reference
- Internal Power-On Reset to Zero Volts
- Asynchronous $\overline{CLR}$ Pin
- Output Buffer Configurable for Gain of 1 or 2
- Parallel 16-Bit or 2-Byte Double Buffered Interface
- Narrow 28-Lead SSOP Package
- Multiplying Capability

APPLICATIONS

- Instrumentation
- Digital Calibration
- Industrial Process Control
- Automatic Test Equipment
- Communication Test Equipment

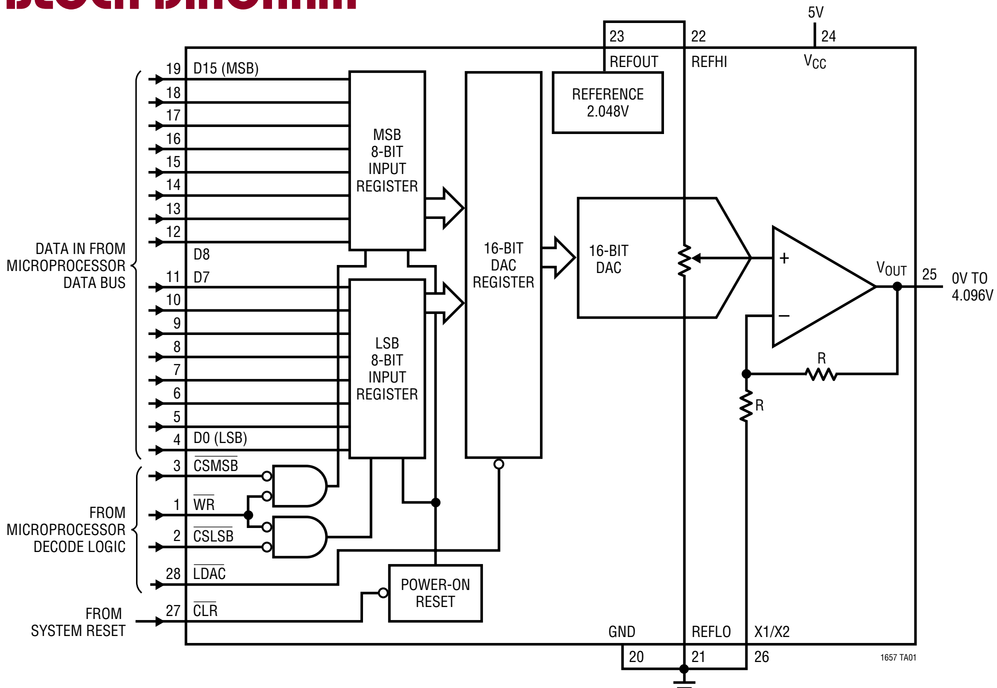
DESCRIPTION

The LTC®1657 is a complete single supply, rail-to-rail voltage output, 16-bit digital-to-analog converter (DAC) in a 28-pin SSOP or PDIP package. It includes a rail-to-rail output buffer amplifier, an internal 2.048V reference and a double buffered parallel digital interface.

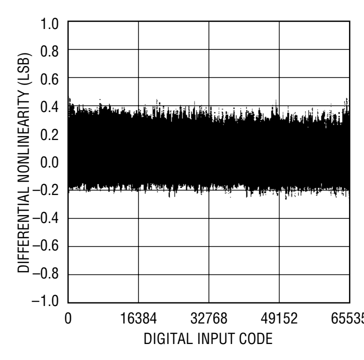
The LTC1657 operates from a 4.5V to 5.5V supply. It has a separate reference input pin that can be driven by an external reference. The full-scale output can be 1 or 2 times the reference voltage depending on how the X1/X2 pin is connected.

The LTC1657 is similar to Linear Technology Corporation's LTC1450 12-bit V_{OUT} DAC family allowing an upgrade path. It is the only buffered 16-bit parallel DAC in a 28-lead SSOP package and includes an onboard reference for stand alone performance.

BLOCK DIAGRAM



Differential Nonlinearity vs Input Code

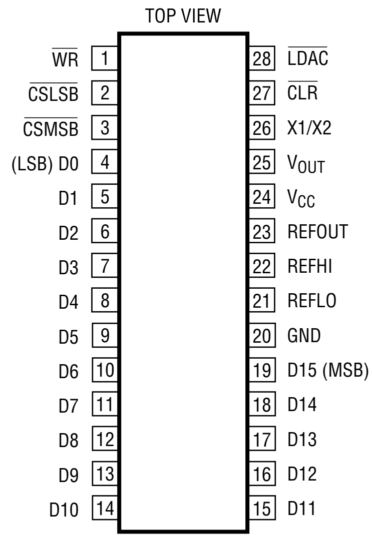


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} to GND .... −0.5V to 7.5V
TTL Input Voltage, REFHI, REFLO,
X1/X2 .... −0.5V to 7.5V
V_{OUT}, REFOUT .... −0.5V to (V_{CC} + 0.5V)
Operating Temperature Range
LTC1657C .... 0°C to 70°C
LTC1657I .... −40°C to 85°C
Maximum Junction Temperature .... 125°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE 28-LEAD PDIP
GN PACKAGE 28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W (G)
T_{JMAX} = 125°C, θ_{JA} = 58°C/W (N)

ORDER PART NUMBER
LTC1657CGN
LTC1657CN
LTC1657IGN
LTC1657IN

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 4.5V to 5.5V, V_{OUT} unloaded, REFOUT tied to REFHI, REFLO tied to GND, X1/X2 tied to GND, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DAC (Note 2)							
	Resolution		●	16			Bits
	Monotonicity		●	16			Bits
DNL	Differential Nonlinearity	Guaranteed Monotonic (Note 3)	●		±0.5	±1.0	LSB
INL	Integral Nonlinearity	(Note 3)	●		±4	±12	LSB
ZSE	Zero Scale Error		●	0		2	mV
V_{OS}	Offset Error	Measured at Code 200	●		±0.3	±3	mV
$V_{OS}TC$	Offset Error Tempco				±5		µV/°C
	Gain Error		●		±2	±16	LSB
	Gain Error Drift				0.5		ppm/°C
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	4.5		5.5	V
I_{CC}	Supply Current	4.5V ≤ V_{CC} ≤ 5.5V (Note 4)	●		650	1200	µA
Op Amp DC Performance							
	Short-Circuit Current Low	V_{OUT} Shorted to GND	●		70	120	mA
	Short-Circuit Current High	V_{OUT} Shorted to V_{CC}	●		80	140	mA
	Output Impedance to GND	Input Code = 0	●		40	120	Ω
	Output Line Regulation	Input Code = 65535, V_{CC} = 4.5V to 5.5V	●			4	mV/V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 4.5V to 5.5V, V_{OUT} unloaded, REFOUT tied to REFHI, REFLO tied to GND, X1/X2 tied to GND, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AC Performance							
	Voltage Output Slew Rate	(Note 5)	●	±0.3	±0.7		V/µs
	Voltage Output Settling Time	(Note 5) to 0.0015% (16-Bit Settling Time) (Note 5) to 0.012% (13-Bit Settling Time)			20 10		µs µs
	Digital Feedthrough				0.3		nV•s
	Midscale Glitch Impulse	DAC Switch Between 8000_H and $7FFF_H$			8		nV•s
	Output Voltage Noise Spectral Density	At 1kHz			250		$nV/\sqrt{Hz}$
Digital I/O							
V_{IH}	Digital Input High Voltage		●	2.4			V
V_{IL}	Digital Input Low Voltage		●			0.8	V
V_{OH}	Digital Output High Voltage		●	V_{CC} – 1			V
V_{OL}	Digital Output Low Voltage		●			0.4	V
I_{LEAK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±10	µA
C_{IN}	Digital Input Capacitance	(Note 6)				10	pF
Switching Characteristics							
t_{CS}	$\overline{CS}$ (MSB or LSB) Pulse Width		●	40			ns
t_{WR}	$\overline{WR}$ Pulse Width		●	40			ns
t_{CWS}	$\overline{CS}$ to $\overline{WR}$ Setup		●	0			ns
t_{CWH}	$\overline{CS}$ to $\overline{WR}$ Hold		●	0			ns
t_{DWS}	Data Valid to $\overline{WR}$ Setup		●	40			ns
t_{DWH}	Data Valid to $\overline{WR}$ Hold		●	0			ns
t_{LDAC}	$\overline{LDAC}$ Pulse Width		●	40			ns
t_{CLR}	$\overline{CLR}$ Pulse Width		●	40			ns
Reference Output (REFOUT)							
	Reference Output Voltage		●	2.036	2.048	2.060	V
	Reference Output Temperature Coefficient				15		ppm/°C
	Reference Line Regulation	V_{CC} = 4.5V to 5.5V	●			±1.5	mV/V
	Reference Load Regulation	Measured at I_{OUT} = 100µA	●			5	mV/A
	Short-Circuit Current	REFOUT Shorted to GND	●		50	100	mA
Reference Input							
	REFHI, REFLO Input Range	(Note 6) See Applications Information X1/X2 Tied to V_{OUT} X1/X2 Tied to GND	 ● ●	 0 0		 V_{CC} – 1.5 V_{CC}/2	 V V
	REFHI Input Resistance		●	16	25		kΩ

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: External reference REFHI = 2.2V. V_{CC} = 5V.

Note 3: Nonlinearity is defined from code 128 to code 65535 (full scale). See Applications Information.

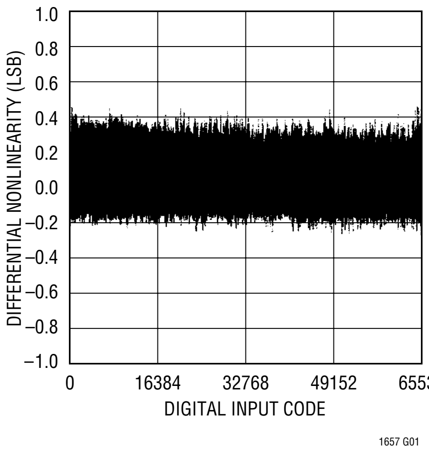
Note 4: Digital inputs at 0V or V_{CC}.

Note 5: DAC switched between all 1s and all 0s.

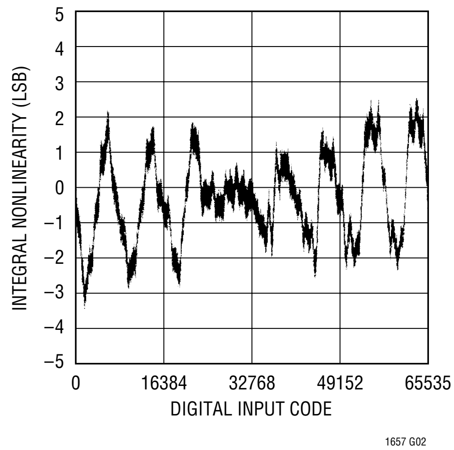
Note 6: Guaranteed by design. Not subject to test.

TYPICAL PERFORMANCE CHARACTERISTICS

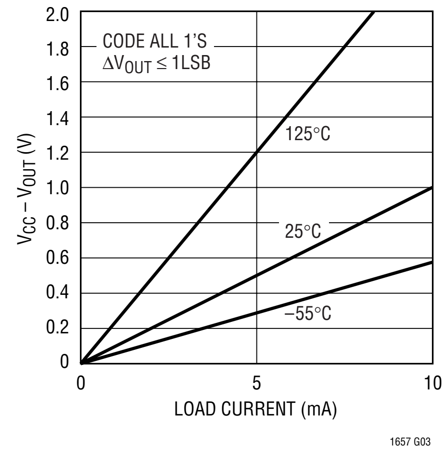
Differential Nonlinearity



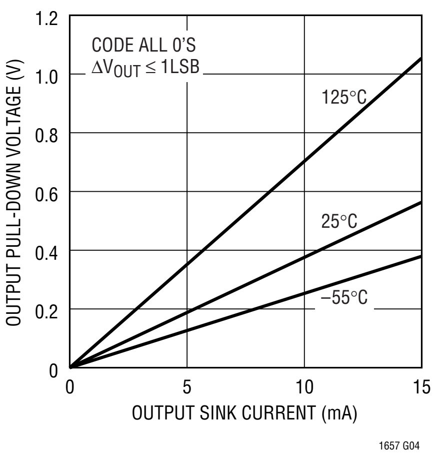
Integral Nonlinearity



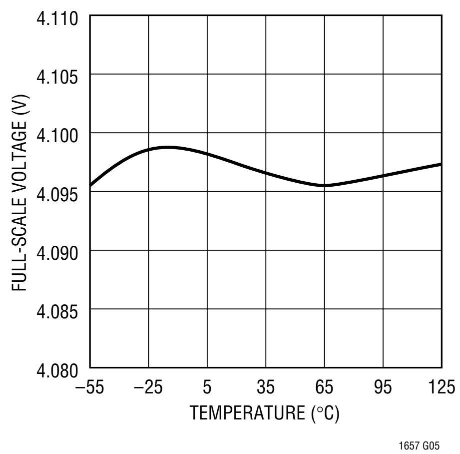
Minimum Supply Headroom for Full Output Swing vs Load Current



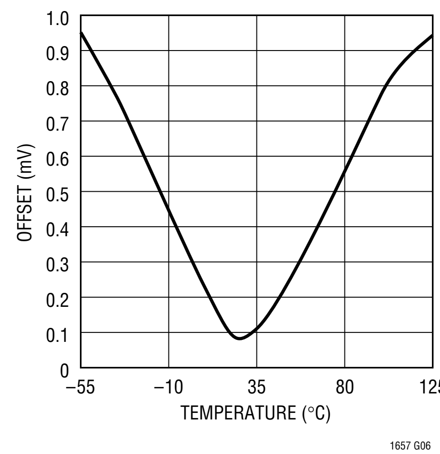
Minimum Output Voltage vs Output Sink Current



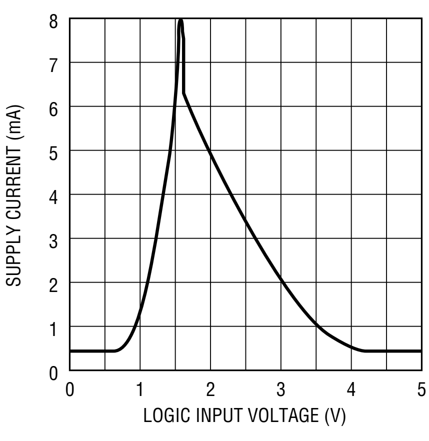
Full-Scale Voltage vs Temperature



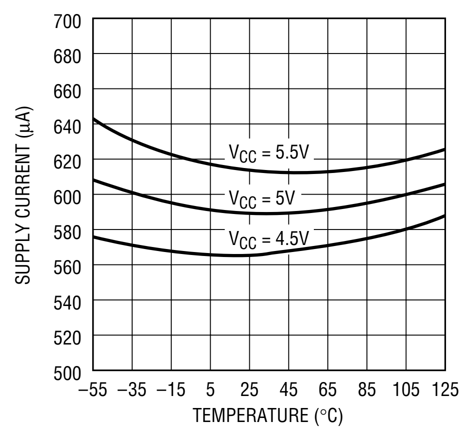
Offset Error vs Temperature



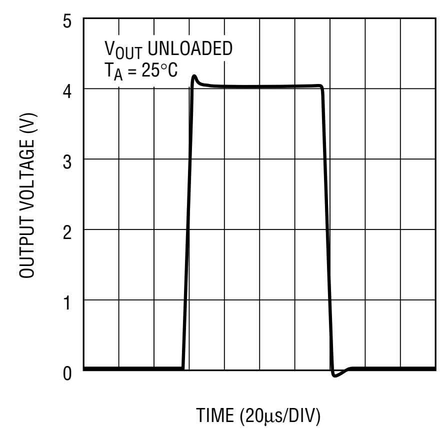
Supply Current vs Logic Input Voltage



Supply Current vs Temperature



Large-Signal Transient Response



PIN FUNCTIONS

$\overline{\text{WR}}$ (Pin 1): Write Input (Active Low). Used with $\overline{\text{CSMSB}}$ and/or $\overline{\text{CSLSB}}$ to control the input registers. While $\overline{\text{WR}}$ and $\overline{\text{CSMSB}}$ and/or $\overline{\text{CSLSB}}$ are held low, data writes into the input register.

$\overline{\text{CSLSB}}$ (Pin 2): Chip Select Least Significant Byte (Active Low). Used with $\overline{\text{WR}}$ to control the LSB 8-bit input registers. While $\overline{\text{WR}}$ and $\overline{\text{CSLSB}}$ are held low, the LSB byte writes into the LSB input register. Can be connected to $\overline{\text{CSMSB}}$ for simultaneous loading of both sets of input latches on a 16-bit bus.

$\overline{\text{CSMSB}}$ (Pin 3): Chip Select Most Significant Byte (Active Low). Used with $\overline{\text{WR}}$ to control the MSB 8-bit input registers. While $\overline{\text{WR}}$ and $\overline{\text{CSMSB}}$ are held low, the MSB byte writes into the MSB input register. Can be connected to $\overline{\text{CSLSB}}$ for simultaneous loading of both sets of input latches on a 16-bit bus.

D0 to D7 (Pins 4 to 11): Input data for the Least Significant Byte. Written into LSB input register when $\overline{\text{WR}}$ = 0 and $\overline{\text{CSLSB}}$ = 0.

D8 to D15 (Pins 12 to 19): Input data for the Most Significant Byte. Written into MSB input register when $\overline{\text{WR}}$ = 0 and $\overline{\text{CSMSB}}$ = 0.

GND (Pin 20): Ground.

REFLO (Pin 21): Lower input terminal of the DAC's internal resistor ladder. Typically connected to Analog Ground. An input code of $(0000)_H$ will connect the positive input of the output buffer to this end of the ladder. Can be used to offset the zero scale above ground.

REFHI (Pin 22): Upper input terminal of the DAC's internal resistor ladder. Typically connected to REFOUT. An input code of $(FFFF)_H$ will connect the positive input of the output buffer to 1LSB below this voltage.

REFOUT (Pin 23): Output of the internal 2.048V reference. Typically connected to REFHI to drive internal DAC resistor ladder.

V_{CC} (Pin 24): Positive Power Supply Input. $4.5V \le V_{CC} \le 5.5V$. Requires a 0.1μF bypass capacitor to ground.

V_{OUT} (Pin 25): Buffered DAC Output.

X1/X2 (Pin 26): Gain Setting Resistor Pin. Connect to GND for G = 2 or to V_{OUT} for G = 1. This pin should always be tied to a low impedance source, such as ground or V_{OUT}, to ensure stability of the output buffer when driving capacitive loads.

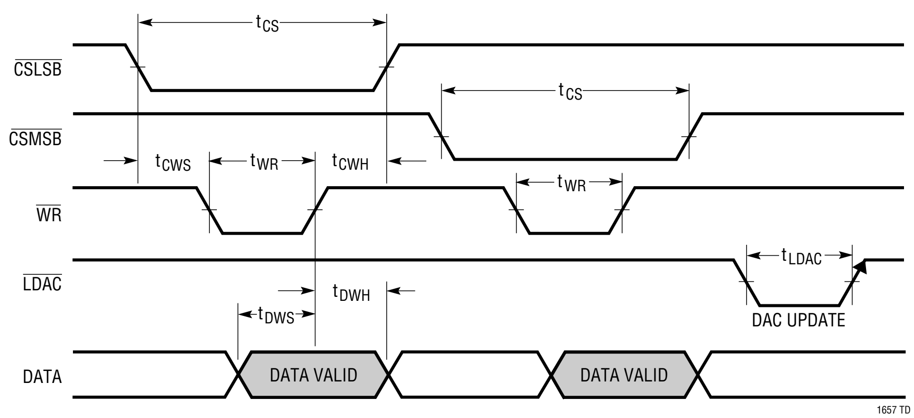
$\overline{\text{CLR}}$ (Pin 27): Clear Input (Asynchronous Active Low). A low on this pin asynchronously resets all input and DAC registers to 0s.

$\overline{\text{LDAC}}$ (Pin 28): Load DAC (Asynchronous Active Low). Used to asynchronously transfer the contents of the input registers to the DAC register which updates the output voltage. If held low, the DAC register loads data from the input registers which will immediately update V_{OUT}.

DIGITAL INTERFACE TRUTH TABLE

$\overline{CLR}$	$\overline{CSMSB}$	$\overline{CSLSB}$	$\overline{WR}$	$\overline{LDAC}$	FUNCTION
L	X	X	X	X	Clears input and DAC registers to zero
H	X	X	X	L	Loads DAC register with contents of input registers
H	X	X	X	H	Freezes contents of DAC register
H	L	H	L	X	Writes MSB byte into MSB input register
H	H	L	L	X	Writes LSB byte into LSB input register
H	L	L	L	X	Writes MSB and LSB bytes into MSB and LSB input registers
H	X	X	H	X	Inhibits write to MSB and LSB input registers
H	H	X	X	X	Inhibits write to MSB input register
H	X	H	X	X	Inhibits write to LSB input register
H	L	L	L	L	Data bus flows directly through input and DAC registers

TIMING DIAGRAM



DEFINITIONS

Resolution (n): Resolution is defined as the number of digital input bits (n). It defines the number of DAC output states (2^n) that divide the full-scale range. Resolution does not imply linearity.

Full-Scale Voltage (V_{FS}): This is the output of the DAC when all bits are set to 1.

Voltage Offset Error (V_{OS}): Normally, the DAC offset is the voltage at the output when the DAC is loaded with all zeros. The DAC can have a true negative offset, but because the part is operated from a single supply, the output cannot go below zero. If the offset is negative, the output will remain near 0V resulting in the transfer curve shown in Figure 1.

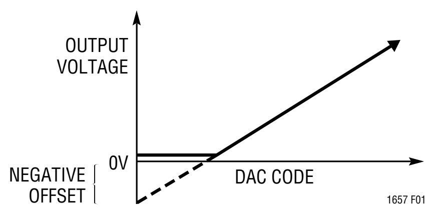


Figure 1. Effect of Negative Offset

The offset of the part is measured at the code that corresponds to the maximum offset specification:

$$V_{OS} = V_{OUT} - [(Code)(V_{FS})/(2^n - 1)]$$

Least Significant Bit (LSB): One LSB is the ideal voltage difference between two successive codes.

$$LSB = (V_{FS} - V_{OS})/(2^n - 1) = (V_{FS} - V_{OS})/65535$$

Nominal LSBs:

LTC1657 LSB = 4.096V/65535 = 62.5µV

DAC Transfer Characteristic:

$$V_{OUT} = G \bullet \left(\frac{REFHI - REFLO}{65536}\right)(CODE) + REFLO$$

G = 1 for X1/X2 connected to V_{OUT}

G = 2 for X1/X2 connected to GND

CODE = Decimal equivalent of digital input ($0 \le CODE \le 65535$)

Zero-Scale Error (ZSE): The output voltage when the DAC is loaded with all zeros. Since this is a single supply part, this value cannot be less than 0V.

Integral Nonlinearity (INL): End-point INL is the maximum deviation from a straight line passing through the end points of the DAC transfer curve. Because the part operates from a single supply and the output cannot go below zero, the linearity is measured between full scale and the code corresponding to the maximum offset specification. The INL error at a given input code is calculated as follows:

$$INL\ (In\ LSBs) = [V_{OUT} - V_{OS} - (V_{FS} - V_{OS})(code/65535)]$$

V_{OUT} = The output voltage of the DAC measured at the given input code

Differential Nonlinearity (DNL): DNL is the difference between the measured change and the ideal one LSB change between any two adjacent codes. The DNL error between any two codes is calculated as follows:

$$DNL = (\Delta V_{OUT} - LSB)/LSB$$

ΔV_{OUT} = The measured voltage difference between two adjacent codes

Digital Feedthrough: The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in nV • s.

OPERATION

Parallel Interface

The data on the input of the DAC is written into the DAC's input registers when Chip Select ($\overline{CSLSB}$ and/or $\overline{CSMSB}$) and $\overline{WR}$ are at a logic low. The data that is written into the input registers will depend on which of the Chip Selects are at a logic low (see Digital Interface Truth Table). If $\overline{WR}$ and $\overline{CSLSB}$ are both low and $\overline{CSMSB}$ is high, then only data on the eight LSBs (D0 to D7) is written into the input registers. Similarly, if $\overline{WR}$ and $\overline{CSMSB}$ are both low and $\overline{CSLSB}$ is high, then only data on the eight MSBs (D8 to D15) is written into the input registers. Data is written into both the Least Significant Data Bits (D0 to D7) and the Most Significant Bits (D8 to D15) at the same time if $\overline{WR}$, $\overline{CSLSB}$ and $\overline{CSMSB}$ are low. If $\overline{WR}$ is high or both $\overline{CSMSB}$ and $\overline{CSLSB}$ are high, then no data is written into the input registers.

Once data is written into the input registers, it can be written into the DAC register. This will update the analog voltage output of the DAC. The DAC register is written by a logic low on $\overline{LDAC}$. The data in the DAC register will be held when $\overline{LDAC}$ is high.

When $\overline{WR}$, $\overline{CSLSB}$, $\overline{CSMSB}$ and $\overline{LDAC}$ are all low, the registers are transparent and data on pins D0 to D15 flows directly into the DAC register.

For an 8-bit data bus connection, tie the MSB byte data pins to their corresponding LSB byte pins (D15 to D7, D14 to D6, etc).

Power-On Reset

The LTC1657 has an internal power-on reset that resets all internal registers to 0's on power-up (equivalent to the $\overline{CLR}$ pin function).

Reference

The LTC1657 includes an internal 2.048V reference, giving the LTC1657 a full-scale range of 4.096V in the gain-of-2 configuration. The onboard reference in the LTC1657 is not internally connected to the DAC's reference resistor string but is provided on an adjacent pin for flexibility. Because the internal reference is not internally connected to the DAC resistor ladder, an external reference can be used or the resistor ladder can be driven by an external source in multiplying applications. The external reference or source must be capable of driving the 16k (minimum) DAC ladder resistance.

Internal reference output noise can be reduced with a bypass capacitor to ground. (Note: The reference does not require a bypass capacitor to ground for nominal operation.) When bypassing the reference, a small value resistor in series with the capacitor is recommended to help reduce peaking on the output. A 10Ω resistor in series with a 4.7µF capacitor is optimum for reducing reference generated noise. Internal reference output voltage noise spectral density at 1kHz is typically $150nV/\sqrt{Hz}$.

DAC Resistor Ladder

The high and low end of the DAC ladder resistor string (REFHI and REFLO, respectively) are not connected internally on this part. Typically, REFHI will be connected to REFOUT and REFLO will be connected to GND. X1/X2 connected to GND will give the LTC1657 a full-scale output swing of 4.096V.

Either of these pins can be driven up to V_{CC} – 1.5V when using the buffer in the gain-of-1 configuration. The resistor string pins can be driven to $V_{CC}/2$ when the buffer is in the gain of 2 configuration. The resistance between these two pins is typically 25k (16k min).

Voltage Output

The output buffer for the LTC1657 can be configured for two different gain settings. By tying the X1/X2 pin to GND, the gain is set to 2. By tying the X1/X2 pin to V_{OUT}, the gain is set to unity.

The LTC1657 rail-to-rail buffered output can source or sink 5mA within 500mV of the positive supply voltage or ground at room temperature. The output stage is equipped with a deglitcher that results in a midscale glitch impulse of 8nV • s. The output swings to within a few millivolts of either supply rail when unloaded and has an equivalent output resistance of 40Ω when driving a load to the rails.

APPLICATIONS INFORMATION

Rail-to-Rail Output Considerations

In any rail-to-rail DAC, the output swing is limited to voltages within the supply range.

If the DAC offset is negative, the output for the lowest codes limits at 0V as shown in Figure 1b.

Similarly, limiting can occur near full scale when the REF pin is tied to $V_{CC}/2$. If $V_{REF} = V_{CC}/2$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC} as shown in Figure 1c. No full-scale limiting can occur if V_{REF} is less than $(V_{CC} – FSE)/2$.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

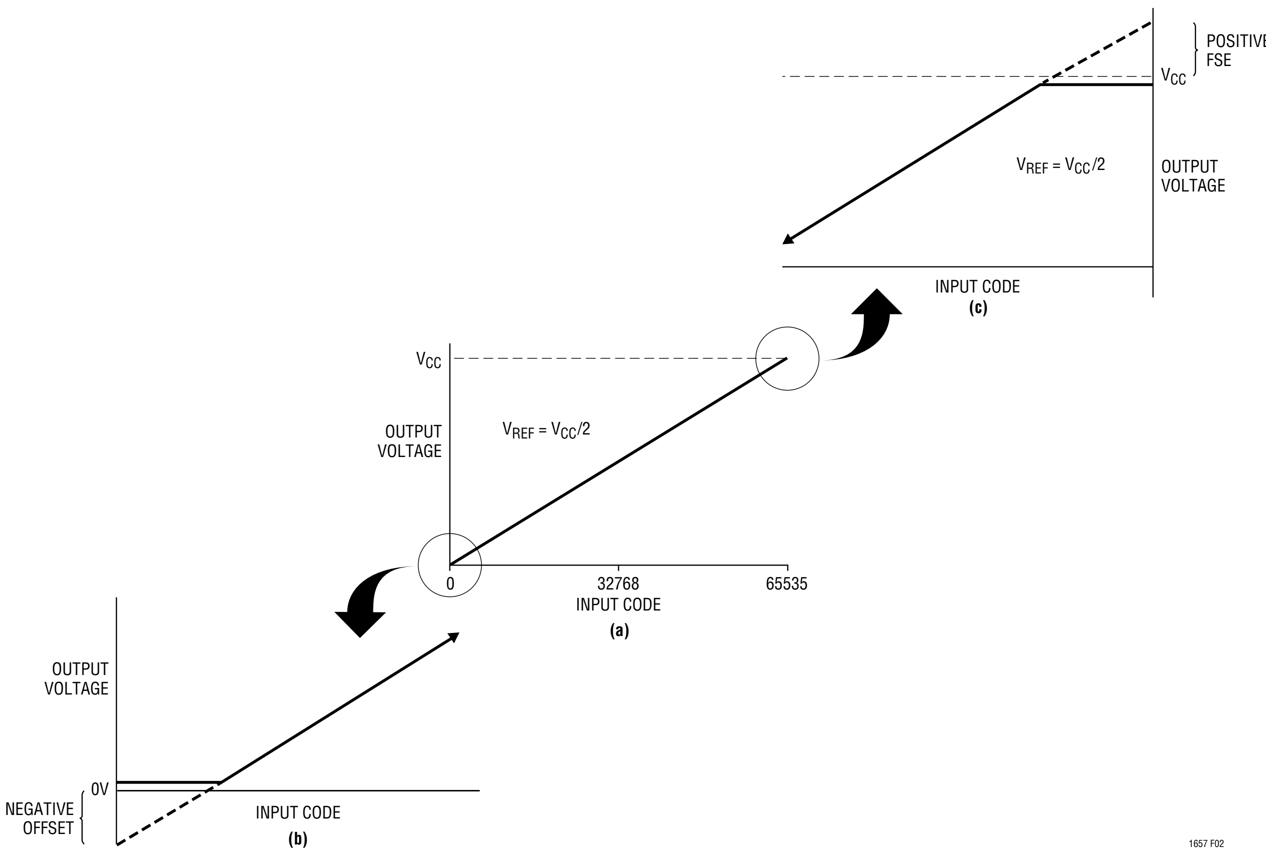
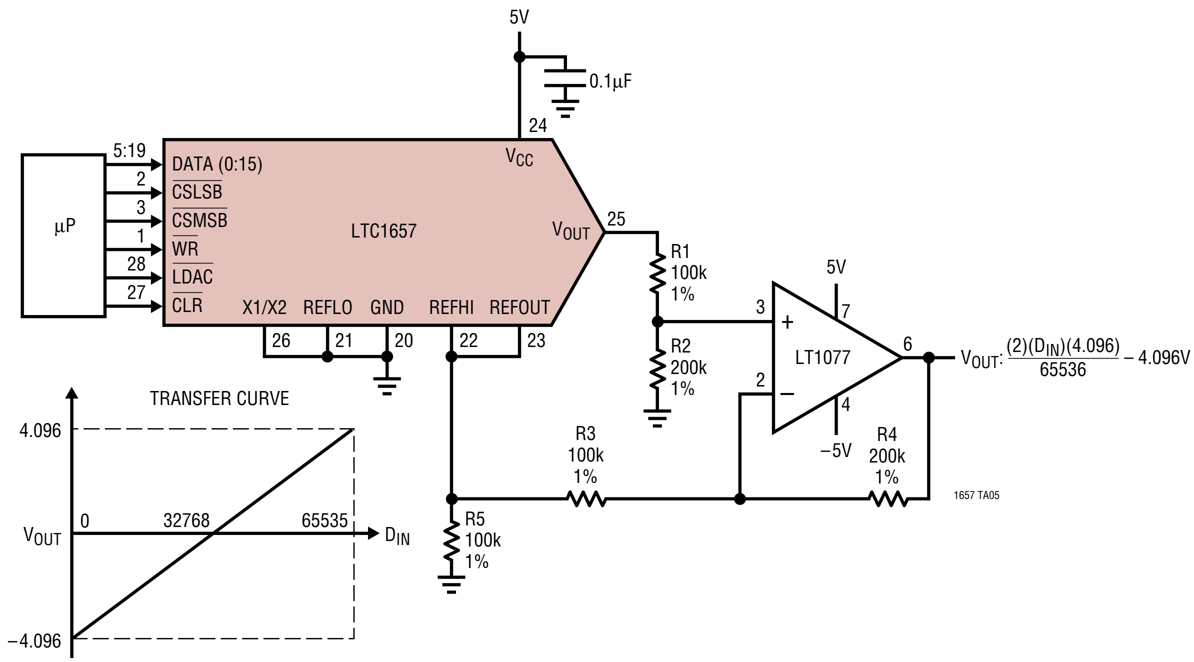


Figure 2. Effects of Rail-to-Rail Operation On a DAC Transfer Curve. (a) Overall Transfer Function (b) Effect of Negative Offset for Codes Near Zero Scale (c) Effect of Positive Full-Scale Error for Input Codes Near Full Scale When $V_{REF} = V_{CC}/2$

TYPICAL APPLICATIONS

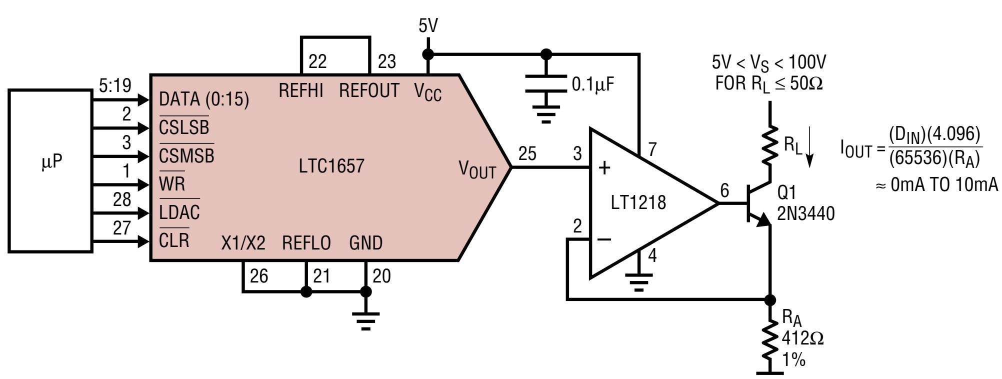
This circuit shows how to make a bipolar output 16-bit DAC with a wide output swing using an LTC1657 and an LT1077. R1 and R2 resistively divide down the LTC1657 output and an offset is summed in using the LTC1657 onboard 2.048V reference and R3 and R4. R5 ensures that the onboard reference is always sourcing current and never has to sink any current even when V_{OUT} is at full scale. The LT1077 output will have a wide bipolar output swing of –4.096V to 4.096V as shown in the figure below. With this output swing, 1LSB = 125µV.

A Wide Swing, Bipolar Output 16-Bit DAC



This circuit shows a digitally programmable current source from an external voltage source using an external op amp, an LT1218 and an NPN transistor (2N3440). Any digital word from 0 to 65535 is loaded into the LTC1657 and its output correspondingly swings from 0V to 4.096V. This voltage will be forced across the resistor R_A. If R_A is chosen to be 412Ω, the output current will range from 0mA at zero scale to 10mA at full scale. The minimum voltage for V_S is determined by the load resistor R_L and Q1's V_{CESAT} voltage. With a load resistor of 50Ω, the voltage source can be 5V.

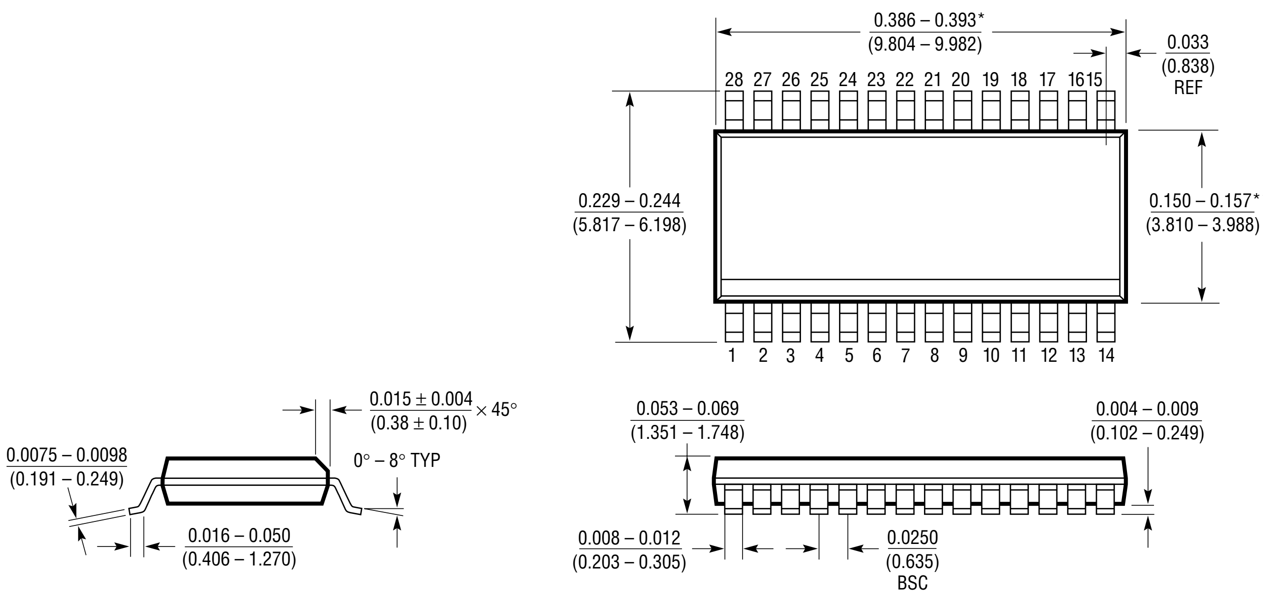
Digitally Programmable Current Source



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

GN Package
28-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)

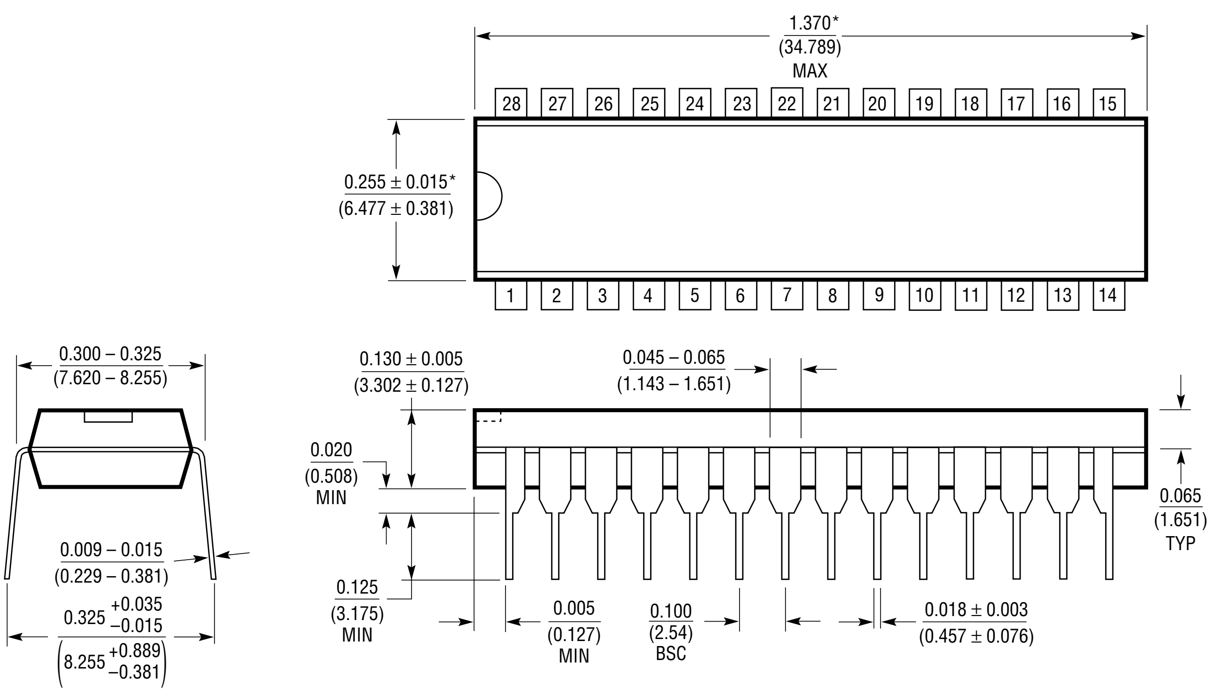


* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN28 (SSOP) 1098

N Package
28-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



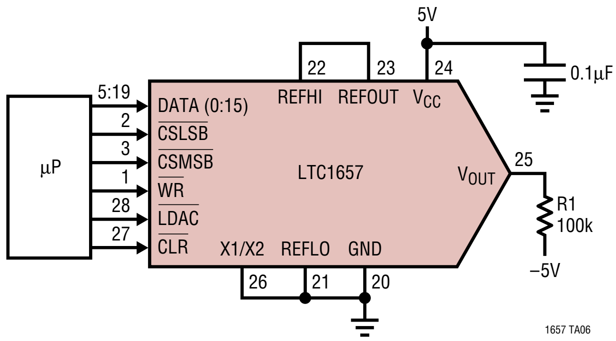
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N28 1098

TYPICAL APPLICATION

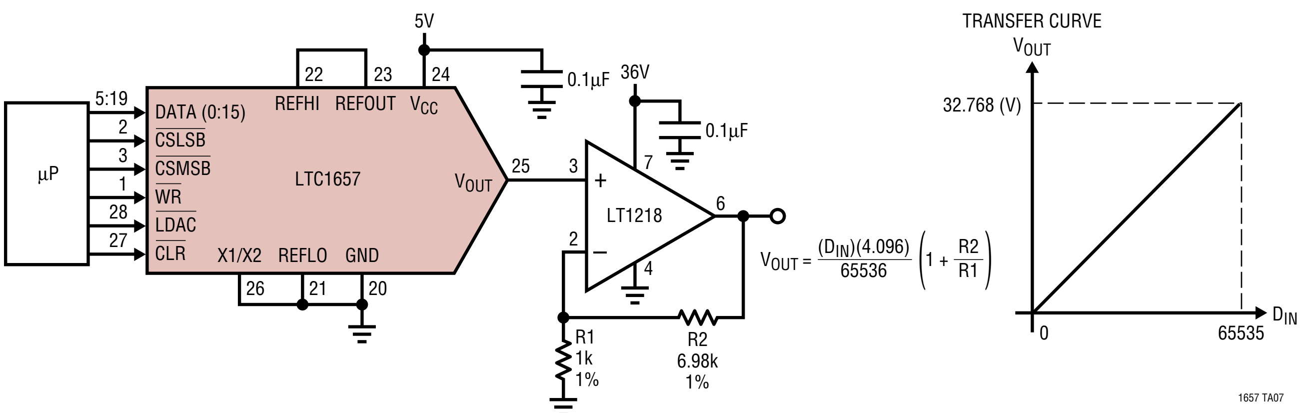
This circuit shows how to measure negative offset. Since LTC1657 operates on a single supply, if its offset is negative, the output for code 0 limits at 0V. To measure this negative offset, a negative supply is needed, connect resistor R1 as shown in the figure. The output voltage is the negative offset when code 0 is loaded in.

Negative Offset Measurement



Although LTC1657 output is up to 4.096V with its internal reference, higher voltages can be achieved with the help of another op amp. The following circuit shows how to increase the output swing of LTC1657 by using an LT1218. As shown in the configuration, the output of LTC1657 is amplified by 8 for an output swing of 0V to 32.768V, or a convenient 0.5mV/LSB.

A Higher Voltage Output DAC



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1446(L)	Dual 12-Bit V_{OUT} DACs in SO-8 Package	V_{CC} = 5V (3V), V_{OUT} = 0V to 4.095V (0V to 2.5V)
LTC1450(L)	Single 12-Bit V_{OUT} DACs with Parallel Interface	V_{CC} = 5V (3V), V_{OUT} = 0V to 4.095V (0V to 2.5V)
LTC1458(L)	Quad 12-Bit Rail-to-Rail Output DACs with Added Functionality	V_{CC} = 5V (3V), V_{OUT} = 0V to 4.095V (0V to 2.5V)
LTC1650	Single 16-Bit V_{OUT} Industrial DAC in 16-Pin SO	V_{CC} = ±5V, Low Power, Deglitched, 4-Quadrant Multiplying V_{OUT}
LTC1655(L)	Single 16-Bit V_{OUT} DAC with Serial Interface in SO-8	V_{CC} = 5V (3V), Low Power, Deglitched, V_{OUT} = 0V to 4.096V (0V to 2.5V)

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